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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,924	09/05/2003	Gregory Tad Kishi	TUC920030091US1	8629

45216 7590 10/25/2005

KUNZLER & ASSOCIATES
8 EAST BROADWAY
SUITE 600
SALT LAKE CITY, UT 84111

EXAMINER	
CAMPOS, YAIMA	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 10/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,924	KISHI, GREGORY TAD	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-10,12-16,18-22 and 24-30* is/are rejected.

7)☒ Claim(s) *5,11,17 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/5/03 and 9/11/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10655924 has a total of 30 claims pending in the application; there are 6 independent claims and 24 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

4. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statements dated September 5, 2003 and September 11, 2003 are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

IV. OBJECTIONS TO THE SPECIFICATION

CLAIM OBJECTIONS

5. Claim 24 is objected to because of the following informalities:

Claim 24 refers to the "method of claim 18." Claim 18 describes a system, not a method; additionally, if claim 24 depended on claim 18, it would be a duplicate of claim 18. It is believed that claim 24 was intended to refer to the "method" of claim 19 and has been treated as such for the rest of this Office action. Accordingly, applicant might consider changing the dependency of claim 24 from claim 18 to claim 19.

Appropriate correction is required.

V. REJECTIONS NOT BASED ON PRIOR ART

a. DEFICIENCIES IN THE CLAIMED SUBJECT MATTER

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 8 recites the limitation "the order used under the second scheme " in line 2. There is insufficient antecedent basis for this limitation in the claim. The applicants might consider amending this claim to read –**an order used under the second scheme**--.

VI. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

8. **Claims 1-3, 6, 19-21 and 24-30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bogin et al. (US 6,658,533) in view of Liu et al. (US 6,922,754).

9. As per **claims 1 and 19**, Bogin discloses an apparatus/system for "flushing data from cache to secondary storage" **[Write cache can flush entries to memory (Figure 3 and Column 4, lines 54-55)]** "comprising an identification module configured to identify predefined high priority cache structures and predefined low priority cache structures." This patent mentions that **[Various criteria can be used to determine which entry in the write cache will be flushed first (Column 5, lines 6-7 and Column 6, lines 4-21)]** and further describes the use of priority criteria for flushing data from cache **[Memory operations can have high or low priority (Column 6, lines 5-45)]**. Bogin further teaches cache flushing based on demand in such a way that high demand for cache space would be **[if the number of entries in write cache storage (291) exceeds a high threshold value, the resulting flushing operations can be assigned to the high priority category (Figures 3 and 5 and Column 6, lines 11-15)]**, and additionally explains a low demand that would occur when **[the number of entries does not exceed the low threshold value (Column 6, line 24) the low priority operations will typically have to wait until all high priority operations have been completed (Column 6, lines 8-10)]**.

Bogin does not disclose expressly a "flushing module configured to selectively flush low priority cache structures according to a first scheme in response to a higher demand load and a second scheme in response to a lower demand load".

Liu discloses a "flushing module configured to selectively flush low priority cache structures according to a first scheme in response to a higher demand load and a second scheme in response to a lower demand load" as it is disclosed that **[One or more policies may be related to flushing cache entries (Column 10, lines 36-37). A policy may indicate how aggressively flushing should be performed (Column 10, lines 41-42)]** and further specifies that **[a policy may indicate the priority with which flushing should be done. A policy may indicate the amount of flushing that should be done during a relatively idle time (Column 10, lines 53-54)].**

(US 6,658,533) by Bogin and (US 6,922,754) by Liu are analogous art because they are from the same field of endeavor of cache memory flushing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to make the cache priority flushing apparatus/system of Bogin flush/replace cache data when there is high demand for cache memory space, but also use a cache flushing policy/scheme to flush when the apparatus/system has low demand or has no demand and is idle; as mentioned by Liu.

The motivation for doing so would have been because Liu teaches that flushing when the apparatus/system is idle in addition to flushing when there is high demand for cache memory improves performance **[(Column 1, lines 61-67)]**. Using priority-based flushing assures that valuable cache entries remain in cache as long as they are

needed and allows them to be replaced when they are no longer needed. Combining this flushing algorithm with idle time flushing will further provide the advantages of flushing during low cache memory demand. Liu further explains that **[flushing the cache during relatively idle times or when the stress on the cache exceeds a threshold or taking other measures improves the performance of the system (Column 1, lines 61-67)]**.

Therefore, it would have been obvious to combine (US 6,922,754) by Liu with (US 6,658,533) by Bogin for the benefit of creating a cache flushing system to obtain the invention as specified in claims 1 and 19.

10. As per **claims 2 and 20**, Bogin teaches cache flushing based on priority, but fails to expressly disclose that "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space."

Lie teaches cache flushing when "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space" as it is disclosed that a system may use different policies to flush data from cache and that these policies may indicate how aggressively flushing should be performed **[(Column 10, lines 41-42)]**.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have different and opposite schemes to flush data from cache when there is high demand and when there is low demand for cache memory space. As

explained by Liu; cache structures may be flushed more aggressively at high demand times and less aggressively at low demand times.

The motivation for doing so would have been; as taught by Liu, that **[flushing the cache during relatively idle times or when the stress on the cache exceeds a threshold or taking other measures improves the performance of the system by reducing the bottleneck to storage (Column 1, lines 41 and 61-67)]** over just aggressively flushing data during a time of high demand.

Therefore, it would have been obvious to combine (US 6,922,754) by Liu with (US 6,658,533) by Bogin for the benefit of creating a cache flushing system to obtain the invention as specified in claims 2 and 20.

11. As per **claims 3 and 21,** Bogin discloses a cache flushing apparatus/system wherein "the higher demand load exists when free space in a cache decreases below a selected free space threshold" **[the number of entries in write cache is checked to see if it exceeds that high threshold value. If it does, the priority for flushing operations can be set at the high priority level (Column 6, lines 31-34)].**

12. As per **claims 6 and 24**, Liu discloses a cache flushing system that "flushes data when a lower demand load comprises substantially no demand" as it is taught that **[flushing the cache during relatively idle times (Column 1, Lines 58-59)]** may be done to improve the general performance of the system.

13. As per **claim 25**, this claim requires "means for identifying predefined high priority cache structures and predefined low priority cache structures; (***page 14, paragraph 0055 of applicant's specification defines the means as the***

identification module 302). **[Bogin teaches this limitation in (Column 6, lines 4-21)]**. Claim 25 further requires "means for selectively flushing low priority cache structures according to a first scheme in response to a higher demand load and a second scheme in response to a lower demand load" (***page 16, paragraph 0063 of applicant's specification defines the means as the flushing module 306***). **[Bogin teaches a "flush dispatcher" in (Figure 3 and column 4, lines 54-55) that meets this limitation]**.

14. As per **claim 26**, Bogin teaches cache flushing based on priority, but fails to expressly disclose that "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space".

Liu teaches "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space" as it is disclosed that a system may use different policies to flush data from cache and that these policies may indicate how aggressively flushing should be performed **[(Column 10, lines 41-42)]**.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have different and opposite schemes to flush data from cache when there is high demand and when there is low demand for cache memory space. As explained by Liu, cache structures may be flushed more aggressively at high demand times and less aggressively at low demand times.

The motivation for doing so would have been; as taught by Liu, that **[flushing the cache during relatively idle times or when the stress on the cache exceeds a threshold or taking other measures improves the performance of the system by reducing the bottleneck to storage (Column 1, lines 41 and 61-67)]** over just aggressively flushing data during a time of high demand.

Therefore, it would have been obvious to combine (US 6,922,754) by Liu with (US 6,658,533) by Bogin for the benefit of creating a cache flushing system to obtain the invention as specified in claim 26.

15. As per **claim 27,** Bogin discloses a cache flushing apparatus/system wherein "the higher demand load exists when free space in a cache decreases below a selected free space threshold" **[the number of entries in write cache is checked to see if it exceeds that high threshold value. If it does, the priority for flushing operations can be set at the high priority level (Column 6, lines 31-34)].**

16. As per **claims 28-30**, claims 28-30 encompass the same scope of the invention as that of claims 1-3 and 19-21 in the form of an article of manufacture comprising a program storage medium readable by a processor and embodying one or more instructions executable by a processor to perform a method of flushing **[The invention can be implemented as instructions stored on a machine-readable medium, which can be red and executed by at least one processor to perform the functions described (Bogin; Column 7, lines 29-32)]**. Therefore claims 28-30 are rejected for the same reasons as stated above with regard to claims 1-3 and 19-21.

17. **Claims 4 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bogin et al. (US 6,658,533) in view of Liu et al. (US 6,922,754) as applied to claims 1-3, 6, 19-21 and 24-30 above, and further in view of Defouw et al. (US 6,742,084).

18. As per **claims 4 and 22**, the combination of Bogin as modified by Liu discloses a cache flushing apparatus/system according to the claimed invention as explained above, but fails to disclose expressly that the apparatus/system includes "a sort module to order the low priority cache structures according to size".

Defouw discloses a cache flushing apparatus/system in which "a sort module is included to order the low priority cache structures according to size". **[Defouw teaches that a data block flushed from the cache will always be the least recently used of all the cached blocks within a given size range (Column 2, lines 56-58 and 61-62)].** Defouw describes a method where data blocks are categorized depending on parameters such as data block size and **[are divided into classes such that all blocks in a given class have the same values of the additional parameters (Column 5, lines 51-53)]** as a method of organizing/sorting cache structures by size.

Bogin, Liu and Defouw are analogous art because they are from the same field of endeavor of cache memory flushing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to further modify the cache priority flushing system of Bogin to flush/replace cache data when there is high demand for cache memory space, but also use a cache flushing policy/scheme to flush when the system has low demand or has no demand and is idle; as mentioned by Liu. It would have also been obvious to use

Defouw's teachings to make the claimed invention include a sorting/organization method to further organize the low and high priority cache structures according to other policies such as least recently used algorithm and size, as described by Defouw and Liu.

The suggestion/ motivation for doing so would have been; as explained by Defouw, to **[maximize cache hit ratio, minimize the overall mean response time, and minimize the bandwidth consumed by the staging activity (Column 3, lines 18-20)]**.

Therefore, it would have been obvious to combine (US 6,922,754) by Liu with (US 6,658,533) by Bogin and further with (US 6,742,084) by Defouw for the benefit of creating a cache flushing system to obtain the invention as specified in claims 4 and 22.

19. **Claims 7-10 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bogin et al. (US 6,658,533) in view of Liu et al. (US 6,922,754) and Defouw et al. (US 6,742,084).

20. As per **claims 7 and 10**, Bogin discloses "an apparatus for flushing data from cache to secondary storage" **[Write cache can flush entries to memory (Figure 3 and Column 4, lines 54-55)]** "comprising a flushing module configured to selectively flush low priority structures." Bogin mentions that **[Various criteria can be used to determine which entry in the write cache will be flushed first. (Column 5, lines 6-7) and (Column 6, lines 4-21)]** and further describes the use of priority criteria for flushing data from cache **[Memory operations can have high or low priority (Column 6, lines 5-45)]**. Bogin further teaches cache flushing based on demand in such a way that high

demand for cache space would be **[if the number of entries in write cache storage (291) exceeds a high threshold value, the resulting flushing operations can be assigned to the high priority category (Figures 3 and 5 and Column 6, lines 11-15)]**, and additionally explains a low demand that would occur when **[the number of entries does not exceed the low threshold value (Column 6, line 24) the low priority operations will typically have to wait until all high priority operations have been completed (Column 6, lines 8-10)]**. Bogin also discloses that **[a pseudo least-recently–used (LRU) mechanism can be used to initiate the flushing operation (Column 5, lines 52-54)].**

Bogin does not disclose expressly configuring a flushing module to "selectively flush low priority cache structures according to a first scheme in response to a higher demand load and a second scheme in response to a lower demand load," nor "a sort module configured to order predefined high priority cache structures and predefined low priority cache structures according to a first criteria and a second criteria" where the first criteria comprises "a least recently used algorithm" and the second criteria comprises "a size algorithm."

Liu discloses cache flushing that may "selectively flush low priority cache structures according to a first scheme in response to a higher demand load and a second scheme in response to a lower demand load" **[One or more policies may be related to flushing cache entries (Column 10, lines 36-37). A policy may indicate how aggressively flushing should be performed (Column 10, lines 41-42)]** and further specifies that **[a policy may indicate the priority with which flushing should**

be done. A policy may indicate the amount of flushing that should be done during a relatively idle time (Column 10, lines 53-54)].

Defouw discloses a "a sort module configured to order predefined high priority cache structures and predefined low priority cache structures according to a first criteria and a second criteria" where the first criteria comprises "a least recently used algorithm" and the second criteria comprises "a size algorithm." **[Cache flushing system in which the data block flushed from the cache will always be the least recently used of all the cached blocks within a given size range (Column 2, lines 56-58 and 61-62)].** Defouw describes a method where data blocks are categorized depending on parameters such as data block size and time a block has been in cache **[are divided into classes such that all blocks in a given class have the same values of the additional parameters (Column 5, lines 51-53)]** as a method of organizing/sorting cache structures by size or by any other parameter.

(US 6,658,533) by Bogin, (US 6,922,754) by Liu and (US 6,742,084) by Defouw are analogous art because they are from the same field of endeavor of cache memory flushing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to further modify the cache priority flushing system of Bogin to flush/replace cache data when there is high demand for cache memory space, but also use a cache flushing policy/scheme to flush when the system has low demand or has no demand and is idle; as mentioned by Liu. It would have also been obvious to use Defouw's teachings to make the claimed invention include a sorting/organization

module to further organize the low and high priority cache structures according to other policies such as least recently used algorithm and size, as described by Defouw and Liu.

The motivation for doing so would have been because Liu teaches that **[flushing the cache during relatively idle times or when the stress on the cache exceeds a threshold or taking other measures improves the performance of the system (Column 1, lines 61-67)]**. Defouw explains that the motivation of having a sorting module is to **[maximize cache hit ratio, minimize the overall mean response time, and minimize the bandwidth consumed by the staging activity (Column 3, lines 18-20)]**.

Therefore, it would have been obvious to combine (US 6,922,754) by Liu with (US 6,658,533) by Bogin and further with (US 6,742,084) by Defouw for the benefit of creating a cache flushing system to obtain the invention as specified in claims 7 and 10.

21. As per **claim 8**, Bogin teaches cache flushing based on priority, but fails to expressly disclose that "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space".

Liu teaches that "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space" as it is taught that a system may use different policies to flush data from cache and that these policies may indicate how aggressively flushing should be performed **[(Column 10, lines 41-42)]**.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have different and opposite schemes to flush data from cache when there is high demand and when there is low demand for cache memory space. As explained by Liu, cache structures may be flushed more aggressively at high demand times and less aggressively at low demand times.

The motivation for doing so would have been; as taught by Liu, that **[flushing the cache during relatively idle times or when the stress on the cache exceeds a threshold or taking other measures improves the performance of the system by reducing the bottleneck to storage (Column 1, lines 41 and 61-67)]** over just aggressively flushing data during a time of high demand.

Therefore, it would have been obvious to combine (US 6,922,754) by Liu with (US 6,658,533) by Bogin for the benefit of creating a cache flushing system to obtain the invention as specified in claim 8.

22. As per **claim 9,** Bogin discloses a cache flushing apparatus/system wherein "the higher demand load exists when free space in a cache decreases below a selected free space threshold" **[the number of entries in write cache is checked to see if it exceeds that high threshold value. If it does, the priority for flushing operations can be set at the high priority level (Column 6, lines 31-34)].**

23. As per **claim 12**, Liu discloses a cache flushing system that "flushes data when a lower demand load comprises substantially no demand" as it is taught that **[flushing the cache during relatively idle times (Column 1, Lines 58-59)]** may be done to improve the general performance of the system.

24. **Claims 13-15 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bogin et al. (US 6,658,533) in view of Liu et al. (US 6,922,754).

25. As per **claim 13**, Bogin discloses "a system for flushing data from cache to secondary storage" **[Write cache can flush entries to memory (Figure 3 and Column 4, lines 54-55)]** "comprising a storage manager configured to transfer data between a host and a plurality of logical volumes corresponding to one or more physical volumes, the logical volumes identified as low priority and high priority" **[address translation logic 293 translates physical addresses into logical addresses, I/O controller24 and memory controller 28 (Figure 3 and Column 4, lines 23-47)]**. This patent mentions that **[Various criteria can be used to determine which entry in the write cache will be flushed first. (Column 5, lines 6-7) and (Column 6, lines 4-21)]** and further describes the use of priority criteria for flushing data from cache **[Memory operations can have high or low priority (Column 6, lines 5-45)]**. Bogin further teaches cache flushing based on demand in such a way that high demand for cache space would be **[if the number of entries in write cache storage (291) exceeds a high threshold value, the resulting flushing operations can be assigned to the high priority category (Figures 3 and 5 and Column 6, lines 11-15)]**, and additionally explains a low demand that would occur when **[the number of entries does not exceed the low threshold value (Column 6, line 24) the low priority operations will typically have to wait until all high priority operations have been completed (Column 6, lines 8-10)]**. Bogin also discloses "a media library to transfer data between a direct access storage device cache configured to cache logical volumes and one or

more physical volumes" **[Write cache 29 can flush entries stored in cache storage 291 (Figure 3 and Column 4, lines 4-5 and 34-47)].** Bogin further discloses "a cache manager configured to manage logical volumes stored in the direct access storage device cache and selectively flush" based on priority **[cache flush dispatcher (292) to dispatch the cache lines to the memory (Bogin; Figure 3 and Column 4, lines 34-47)]**.

Bogin does not disclose expressly flushing "low priority logical volumes according to a first scheme in response to higher demand load and a second scheme in response to a lower demand load."

Liu discloses flushing "low priority logical volumes according to a first scheme in response to higher demand load and a second scheme in response to a lower demand load." **[One or more policies may be related to flushing cache entries (Column 10, lines 36-37). A policy may indicate how aggressively flushing should be performed (Column 10, lines 41-42)]** and further specifies that **[a policy may indicate the priority with which flushing should be done. A policy may indicate the amount of flushing that should be done during a relatively idle time (Column 10, lines 53-54)]**.

(US 6,658,533) by Bogin and (US 6,922,754) by Liu are analogous art because they are from the same field of endeavor of cache memory flushing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to make the cache priority flushing apparatus/system of Bogin flush/replace cache data when there is high demand for cache memory space, but also

use a cache flushing policy/scheme to flush when the apparatus/system has low demand or has no demand and is idle; as mentioned by Liu.

The motivation for doing so would have been because Liu teaches that flushing when the apparatus/system is idle in addition to flushing when there is high demand for cache memory improves performance **[(Column 1, lines 61-67)]**. Using priority-based flushing assures that valuable cache entries remain in cache as long as they are needed and allows them to be replaced when they are no longer needed. Combining this flushing algorithm with idle time flushing will further provide the advantages of flushing during low cache memory demand. Liu further explains that **[flushing the cache during relatively idle times or when the stress on the cache exceeds a threshold or taking other measures improves the performance of the system (Column 1, lines 61-67)]**.

Therefore, it would have been obvious to combine (US 6,922,754) by Liu with (US 6,658,533) by Bogin for the benefit of creating a cache flushing system to obtain the invention as specified in claim 13.

26. As per **claim 14**; Bogin teaches cache flushing based on priority, but fails to expressly disclose that "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space".

Liu teaches a cache flushing system in which "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space" as it is taught that a system may use

different policies to flush data from cache and that these policies may indicate how aggressively flushing should be performed **[Column 10, lines 41-42]**.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have different and opposite schemes to flush data from cache when there is high demand and when there is low demand for cache memory space. As explained by Liu, cache structures may be flushed more aggressively at high demand times and less aggressively at low demand times.

The motivation for doing so would have been; as taught by Liu, that **[flushing the cache during relatively idle times or when the stress on the cache exceeds a threshold or taking other measures improves the performance of the system by reducing the bottleneck to storage (Column 1, lines 41 and 61-67)]** over just aggressively flushing data during a time of high demand.

Therefore, it would have been obvious to combine (US 6,922,754) by Liu with (US 6,658,533) by Bogin for the benefit of creating a cache flushing system to obtain the invention as specified in claim 14.

27. As per **claim 15,** Bogin discloses a cache flushing apparatus/system wherein "the higher demand load exists when free space in a cache decreases below a selected free space threshold" **[the number of entries in write cache is checked to see if it exceeds that high threshold value. If it does, the priority for flushing operations can be set at the high priority level (Column 6, lines 31-34)].**

28. As per **claim 18**, Liu discloses a cache flushing system that "flushes data when a lower demand load comprises substantially no demand" as it is taught that **[flushing**

the cache during relatively idle times (Column 1, Lines 58-59)] may be done to improve the general performance of the system.

29. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over Bogin et al. (US 6,658,533) in view of Liu et al. (US 6,922,754) as applied to claims 13-15 and 18 above, and further in view of Defouw et al. (US 6,742,084).

30. As per **claim 16**, as dependent on claim 1, the combination of Bogin as modified by Liu discloses a cache flushing apparatus/system according to the claimed invention as explained above, but fails to disclose expressly that the apparatus/system includes "a sort module to order the low priority cache structures according to size".

Defouw discloses a cache flushing apparatus/system in which "a sort module is included to order the low priority cache structures according to size". **[Defouw teaches that a data block flushed from the cache will always be the least recently used of all the cached blocks within a given size range (Column 2, lines 56-58 and 61-62)].** Defouw describes a method where data blocks are categorized depending on parameters such as data block size and **[are divided into classes such that all blocks in a given class have the same values of the additional parameters (Column 5, lines 51-53)]** as a method of organizing/sorting cache structures by size.

Bogin, Liu and Defouw are analogous art because they are from the same field of endeavor of cache memory flushing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to further modify the cache priority flushing system of Bogin to flush/replace cache data when there is high demand for cache memory space, but also

use a cache flushing policy/scheme to flush when the system has low demand or has no demand and is idle; as mentioned by Liu. It would have also been obvious to use Defouw's teachings to make the claimed invention include a sorting/organization method to further organize the low and high priority cache structures according to other policies such as least recently used algorithm and size, as described by Defouw and Liu

The suggestion/ motivation for doing so would have been; as explained by Defouw, to **[maximize cache hit ratio, minimize the overall mean response time, and minimize the bandwidth consumed by the staging activity (Column 3, lines 18-20)]**.

Therefore, it would have been obvious to combine (US 6,922,754) by Liu with (US 6,658,533) by Bogin and further with (US 6,742,0847) by Defouw for the benefit of creating a cache flushing system to obtain the invention as specified in claim 16.

31. **Claims 1-3, 6, 19-21 and 24-30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Liedberg (US 5,943,687) in view of Loechel (US 5,895,488).

32. As per **claims 1 and 19**, Liedberg discloses "an apparatus for flushing data from a cache to secondary storage" **[invention relates to cache memories, and more particularly to strategies for selecting data to be replaced in cache memory (Column 1, lines 5-7)]** "comprising an identification module configured to identify predefined high priority cache structures and predefined low priority cache structures" **["the cache entry to be replaced is determined by analyzing the priority values to determine the lowest priority value. Then, one of the data items that has the**

lowest priority value is selected and replaced by a replacement data item" in step 405, it is further explained that "the data cache controller 109 additionally employs the inventive data replacement techniques" (Figures 2, 5, 7, Column 9, lines 7-29, Column 3, lines 17-22 and Column 5, lines 53-57)]. Liedberg also discloses "a flushing module configured to selectively flush low priority cache structures" **["the flow of data into and out of the data cache 105 is directed by a data cache controller" and further explains how cache replacement/flushing takes place (Figure 4, Column 4, lines 21-23 and Columns 8-9, lines 63 and 1-29)]**.

Liedberg does not disclose expressly "flushing low priority cache structures according to a first scheme in response to a higher demand load and a second scheme in response to a lower demand load".

Loechel discloses "flushing low priority cache structures according to a first scheme in response to a higher demand load and a second scheme in response to a lower demand load" **["the cache is flushed if the determined percentage of dirty lines exceeds a predetermined threshold" (Abstract, lines 3-4)].** This condition would encompass a period of high demand for cache space. Loechel also teaches that **[if the state of the system is determined to be idle, a line of cache is flushed (Abstract, lines 10-12)]**; providing flushing during a low demand period. Loechel also discloses the existence of a scheme called **["panic flush" when the "amount of dirty cache lines exceeds a predetermined threshold" which equals a period of high demand and of another scheme "one flush line at a time" as disclosed in the invention, which is carried out at idle or low demand periods and is referred to as**

"controlled flushes" (Column 4, lines 57-60)]; providing different schemes of flushing the cache depending on the demand for cache space.

(US 5,943,687) by Liedberg and (US 5,895,488) by Loechel are analogous art because they are from the same field of endeavor of cache memory replacement or flushing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to make the cache priority flushing system of Liedberg flush/replace cache data when there is high demand for cache memory space, but also add the feature of flushing when the system has low demand or has no demand and is idle; as explained by Loechel.

The motivation for doing so would have been; as explained by Loechel, that flushing during idle time also **[minimizes the frequency of cache line flushes initiated by a replacement algorithm so that I/O requests do not have to wait for dirty data in the cache to be written to mass storage and that idle time flushing minimizes the possibility of data loss and performs cache line flushes at an optimal time (Column 4, lines 48-56)]**.

Therefore, it would have been obvious to combine (US 5,895,488) by Loechel with (US 5,943,687) by Liedberg for the benefit of a cache flushing system to obtain the invention as specified in claims 1 and 19.

33. As per **claims 2 and 20**, Liedberg teaches cache flushing based on priority, but fails to expressly discloses that "the selection criteria for a scheme used when there is

low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space."

Loechel teaches "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space" as it is taught that **[the cache is flushed if the determined percentage of dirty lines exceeds a predetermined threshold (Abstract, lines 3-4)]**. This condition would encompass a high demand for cache space. Loechel also teaches that **[if the state of the system is determined to be idle, a line of cache is flushed (Abstract, lines 10-12)]**; providing flushing during a low demand period, which encompasses no demand since the state of the system would be idle. Loechel also discloses the existence of a scheme called **["panic flush" when the "amount of dirty cache lines exceeds a predetermined threshold" which equals a period of high demand and of another scheme "one flush line at a time" as disclosed in the invention, which is carried out at idle or low demand periods "and is referred to as controlled flushes" (Column 4, lines 57-60)]**; providing different and opposite schemes for flushing the cache depending on the demand for cache space.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have different and opposite schemes to flush data from cache when there is high demand and when there is low demand for cache memory space. As explained by Loechel; cache structures may be flushed with a high intensity; a "panic flush" during high demand or one line at a time; "controlled flushes" during idle times.

The motivation for doing so would have been because Loechel teaches that flushing during idle times **[minimizes the frequency of cache line flushes initiated by a replacement algorithm so that I/O requests do not have to wait for dirty data in the cache to be written to mass storage and that idle time flushing minimizes the possibility of data loss and performs cache line flushes at an optimal time (Column 4, lines 48-56)]**.

Therefore, it would have been obvious to combine (US 5,895,488) by Loechel with (US 5,943,687) by Liedberg for the benefit of a cache flushing system to obtain the invention as specified in claims 2 and 20.

34. As per **claims 3 and 21,** Loechel discloses a cache flushing apparatus/system wherein "the higher demand load exists when free space in a cache decreases below a selected free space threshold" **["the cache is flushed when the amount of dirty cache lines exceeds a predetermined threshold" (Column 4, lines 57-59)]**.

35. As per **claims 6 and 24**, Loechel discloses a cache flushing system that "flushes data when a lower demand load comprises substantially no demand" as it is taught that **[flushing a dirty line when the system is determined to be idle (Column 3, lines 38-40)]** may be done to improve the general performance of the system.

36. As per **claim 25**, this claim requires "means for identifying predefined high priority cache structures and predefined low priority cache structures; (***page 14, paragraph 0055 of applicant's specification defines the means as the identification module 302***). **[Liedberg teaches this limitation as "the cache entry to be replaced is determined by analyzing the priority values to determine the**

lowest priority value. Then, one of the data items that has the lowest priority value is selected and replaced by a replacement data item in step 405;" it is further explained that "the data cache controller 109 additionally employs the inventive data replacement techniques" described above (Figures 2, 5, 7, Column 9, lines 7-29, Column 5, lines 53-57 and Column 3, lines 17-22)]. Claim 25 further requires "means for selectively flushing low priority cache structures according to a first scheme in response to a higher demand load and a second scheme in response to a lower demand load" (***page 16, paragraph 0063 of applicant's specification defines the means as the flushing module 306***). **[Liedberg teaches as "the flow of data into and out of the data cache 105 is directed by a data cache controller" and further explains how cache replacement/flushing takes place (Figure 4, Column 4, lines 21-23 and Columns 8-9, lines 63 and 1-29)]**.

37. As per **claim 26**, Liedberg teaches cache flushing based on priority, but fails to expressly discloses that "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space."

Loechel teaches "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space" as it is taught that **[the cache is flushed if the determined percentage of dirty lines exceeds a predetermined threshold (Abstract, lines 3-4)]**. This condition would encompass a high demand for cache space. Loechel also teaches that **[if the state of the system is determined to be idle, a line of cache is flushed**

(Abstract, lines 10-12)]; providing flushing during a low demand period, which encompasses no demand since the state of the system would be idle. Loechel also discloses the existence of a scheme called **["panic flush" when the "amount of dirty cache lines exceeds a predetermined threshold" which equals a period of high demand and of another scheme "one flush line at a time" as disclosed in the invention, which is carried out at idle or low demand periods "and is referred to as controlled flushes" (Column 4, lines 57-60)]**; providing different and opposite schemes for flushing the cache depending on the demand for cache space.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have different and opposite schemes to flush data from cache when there is high demand and when there is low demand for cache memory space. As explained by Loechel; cache structures may be flushed with a high intensity; a "panic flush" during high demand or one line at a time; "controlled flushes" during idle times.

The motivation for doing so would have been because Loechel teaches that flushing during idle times **[minimizes the frequency of cache line flushes initiated by a replacement algorithm so that I/O requests do not have to wait for dirty data in the cache to be written to mass storage and that idle time flushing minimizes the possibility of data loss and performs cache line flushes at an optimal time (Column 4, lines 48-56)]**.

Therefore, it would have been obvious to combine (US 5,895,488) by Loechel with (US 5,943,687) by Liedberg for the benefit of a cache flushing system to obtain the invention as specified in claim 26.

38. As per **claim 27,** Loechel discloses a cache flushing apparatus/system wherein "the higher demand load exists when free space in a cache decreases below a selected free space threshold" **["the cache is flushed when the amount of dirty cache lines exceeds a predetermined threshold" (Column 4, lines 57-59)].**

39. As per **claims 28-30**, claims 28-30 encompass the same scope of the invention as that of claims 1-3 and 19-21 in the form of an article of manufacture comprising a program storage medium readable by a processor and embodying one or more instructions executable by a processor to perform a method of flushing **[Liedberg discloses that the computer system embodying his invention "executes instructions stored in main memory" and therefore teaches this limitation (Column 4, lines 5-9)]**. Therefore claims 28-30 are rejected for the same reasons as stated above with regard to claims 1-3 and 19-21.

40. **Claims 4 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Liedberg (US 5,943,687) in view of Loechel (US 5,895,488) as applied to claims 1-3, 6, 19-21 and 24-30 above, and further in view of Defouw et al. (US 6,742,084).

41. As per **claims 4 and 22**, the combination of Liedberg as modified by Loechel discloses a cache flushing apparatus/system according to the claimed invention as explained above, but fails to disclose expressly that the apparatus/system includes "a sort module to order the low priority cache structures according to size".

Defouw discloses a cache flushing apparatus/system in which "a sort module is included to order the low priority cache structures according to size". **[Defouw teaches that a data block flushed from the cache will always be the least recently used of**

all the cached blocks within a given size range (Column 2, lines 56-58 and 61-62)].

Defouw describes a method where data blocks are categorized depending on parameters such as data block size and **[are divided into classes such that all blocks in a given class have the same values of the additional parameters (Column 5, lines 51-53)]** as a method of organizing/sorting cache structures by size or by any other parameter.

Liedberg, Loechel and Defouw are analogous art because they are from the same field of endeavor of cache memory flushing.

The motivation for doing so would have been because Defouw teaches that the motivation of having a sorting module is to **[maximize cache hit ratio, minimize the overall mean response time, and minimize the bandwidth consumed by the staging activity (Column 3, lines 18-20)]**.

Therefore, it would have been obvious to combine (US 5,943,687) by Liedberg with (US 5,895,488) by Loechel and further with (US 6,742,084) by Defouw for the benefit of creating a cache flushing system to obtain the invention as specified in claims 4 and 22.

42. **Claims 7-10 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Liedberg (US 5,943,687) in view of Loechel (US 5,895,488), and further in view of Defouw (US 6,742,084).

43. As per **claims 7 and 10**, Liedberg discloses " a flushing module configured to selectively flush low priority cache structures" **["one of the data items that has the lowest priority value is selected and replaced by a replacement data item"**

(Column 3, lines 21-22); it is further explained that "the flow of data into and out of the data cache 105 is directed by a data cache controller" (Figure 4, Column 4, lines 21-23 and Columns 8-9, lines 63 and 1-29).

Liedberg does not disclose expressly configuring a flushing module to "selectively flush low priority cache structures according to a first scheme in response to a higher demand load and a second scheme in response to a lower demand load," nor "a sort module configured to order predefined high priority cache structures and predefined low priority cache structures according to a first criteria and a second criteria" where the first criteria comprises "a least recently used algorithm" and the second criteria comprises "a size algorithm."

Loechel discloses "flushing low priority cache structures according to a first scheme in response to a higher demand load and a second scheme in response to a lower demand load" **[the cache is flushed if the determined percentage of dirty lines exceeds a predetermined threshold (Abstract, lines 3-4)].** This condition would encompass a high demand for cache space. Loechel also teaches that **[if the state of the system is determined to be idle, a line of cache is flushed (Abstract, lines 10-12)]**; providing flushing during a low demand period. Loechel also discloses the existence of a scheme called **["panic flush" when the "amount of dirty cache lines exceeds a predetermined threshold" which equals a period of high demand and of another scheme "one flush line at a time" as disclosed in the invention, which is carried out at idle or low demand periods (Column 4, lines 57-60)]**; providing different schemes of flushing the cache depending on the demand for cache space.

Defouw discloses a "a sort module configured to order predefined high priority cache structures and predefined low priority cache structures according to a first criteria and a second criteria" where the first criteria comprises "a least recently used algorithm" and the second criteria comprises "a size algorithm." **[cache flushing system in which the data block flushed from the cache will always be the least recently used of all the cached blocks within a given size range (Column 2, lines 56-58 and 61-62)].** Defouw describes a method where data blocks are categorized depending on parameters such as data block size and time a block has been in cache **[are divided into classes such that all blocks in a given class have the same values of the additional parameters (Column 5, lines 51-53)]** as a method of organizing/sorting cache structures by size or by any other parameter.

(US 5,943,687) by Liedberg, (US 5,895,488) by Loechel and (US 6,742,084) by Defouw are analogous art because they are from the same field of endeavor of cache memory flushing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to further modify the cache priority flushing system of Liedberg to flush/replace cache data when there is high demand for cache memory space, but also use a cache flushing policy/scheme to flush when the system has low demand or has no demand and is idle; as mentioned by Loechel. It would have also been obvious to use Defouw's teachings to make the claimed invention include a sorting/organization module to further organize the low and high priority cache structures according to other policies such as least recently used algorithm and size, as described by Defouw.

The motivation for doing so would have been because Loechel teaches that flushing during idle times **[minimizes the frequency of cache line flushes initiated by a replacement algorithm so that I/O requests do not have to wait for dirty data in the cache to be written to mass storage and that idle time flushing minimizes the possibility of data loss and performs cache line flushes at an optimal time (Column 4, lines 48-56)]**. Defouw explains that the motivation of having a sorting module is to **[maximize cache hit ratio, minimize the overall mean response time, and minimize the bandwidth consumed by the staging activity (Column 3, lines 18-20)]**.

Therefore, it would have been obvious to combine (US 5,943,687) by Liedberg with (US 5,895,488) by Loechel and further with (US 6,742,084) by Defouw for the benefit of creating a cache flushing system to obtain the invention as specified in claims 7 and 10.

44. As per **claim 8**, Liedberg teaches cache flushing based on priority, but fails to expressly discloses that "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space."

Loechel teaches "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space" as it is taught that **[the cache is flushed if the determined percentage of dirty lines exceeds a predetermined threshold (Abstract, lines 3-4)]**. This condition would encompass a high demand for cache space. Loechel also teaches

that **[if the state of the system is determined to be idle, a line of cache is flushed (Abstract, lines 10-12)]**; providing flushing during a low demand period, which encompasses no demand since the state of the system would be idle. Loechel also discloses the existence of a scheme called **["panic flush" when the "amount of dirty cache lines exceeds a predetermined threshold" which equals a period of high demand and of another scheme "one flush line at a time" as disclosed in the invention, which is carried out at idle or low demand periods "and is referred to as controlled flushes" (Column 4, lines 57-60)]**; providing different and opposite schemes for flushing the cache depending on the demand for cache space.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have different and opposite schemes to flush data from cache when there is high demand and when there is low demand for cache memory space. As explained by Loechel; cache structures may be flushed with a high intensity; a "panic flush" during high demand or one line at a time; "controlled flushes" during idle times.

The motivation for doing so would have been because Loechel teaches that flushing during idle times **[minimizes the frequency of cache line flushes initiated by a replacement algorithm so that I/O requests do not have to wait for dirty data in the cache to be written to mass storage and that idle time flushing minimizes the possibility of data loss and performs cache line flushes at an optimal time (Column 4, lines 48-56)]**.

Therefore, it would have been obvious to combine (US 5,895,488) by Loechel with (US 5,943,687) by Liedberg for the benefit of a cache flushing system to obtain the invention as specified in claim 8.

45. As per **claim 9,** Loechel discloses a cache flushing apparatus/system wherein "the higher demand load exists when free space in a cache decreases below a selected free space threshold" **["the cache is flushed when the amount of dirty cache lines exceeds a predetermined threshold" (Column 4, lines 57-59)].**

46. As per **claim 12**, Loechel discloses a cache flushing system that "flushes data when a lower demand load comprises substantially no demand" as it is taught that **["flushing a dirty line when the system is determined to be idle" (Column 3, lines 38-40)]** may be done to improve the general performance of the system.

47. **Claims 13-15 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Liedberg (US 5,943,687) in view of Loechel (US 5,895,488).

As per **claim 13**, Liedberg discloses "a system for flushing data from cache to secondary storage" **[invention relates to cache memories, and more particularly to strategies for selecting data to be replaced in cache memory (Column 1, lines 5-7)]** "comprising a storage manager configured to transfer data" **[In order to allow the CPU 101 to more quickly retrieve and store data, a data cache 105 is also interposed between the CPU 101 and the main memory 107 (Column 4, lines 18-20)]** "a media library to transfer data between a direct access storage device cache configured to cache" **[Main memory 107, data cache 105 and the bus connecting both (Figure 1 and Column 4, lines 19-25)]**. Liedberg also discloses "a cache

manager configured to manage direct access storage device cache and selectively flush" based on priority **["one of the data items that has the lowest priority value is selected and replaced by a replacement data item" (Column 3, lines 21-22); it is further explained that "the flow of data into and out of the data cache 105 is directed by a data cache controller" (Figure 4, Column 4, lines 21-23 and Columns 8-9, lines 63 and 1-29)]**.

Liedberg does not disclose expressly flushing "low priority logical volumes according to a first scheme in response to higher demand load and a second scheme in response to a lower demand load;" nor it is disclosed the use of "virtual or logical memory space" for the implementation of cache.

Loechel discloses flushing "low priority logical volumes according to a first scheme in response to higher demand load and a second scheme in response to a lower demand load;" **[the cache is flushed if the determined percentage of dirty lines exceeds a predetermined threshold (Abstract, lines 3-4)].** This condition would encompass a high demand for cache space. Loechel also teaches that **[if the state of the system is determined to be idle, a line of cache is flushed (Abstract, lines 10-12)]**; providing flushing during a low demand period. Loechel also discloses the existence of a scheme called **["panic flush" when the "amount of dirty cache lines exceeds a predetermined threshold" which equals a period of high demand and of another scheme "one flush line at a time" as disclosed in the invention, which is carried out at idle or low demand periods (Column 4, lines 57-60)]**; providing different schemes of flushing the cache depending on the demand for cache space.

Loechel also discloses the use of "virtual or logical volumes" for he implementation of the cache **[The volume identifier field 336 may include information which identifies the volume (i.e., the logical section of a disk array) to which the cache line 214 belongs (Column 6, lines 23-26) and the logical structure of an exemplary cache (Figure 2) and high level diagram for a computer system which shows a direct access memory 106, a cache, and an I/O management controller (Figure 1)]**.

(US 5,943,687) by Liedberg and (US 5,895,488) by Loechel are analogous art because they are from the same field of endeavor of cache memory flushing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to further modify the cache priority flushing system of Liedberg to flush/replace cache data when there is high demand for cache memory space, but also use a cache flushing policy/scheme to flush when the system has low demand or has no demand and is idle; as mentioned by Loechel. It would have also been obvious to use a logical or virtual cache implementation as explained by Loechel and to make all the cache structures such as the storage manager, library manager and cache manager include functionality to use virtual addressing for the cache flushing system disclosed by Applicant.

The motivation for doing so would have been because Loechel teaches that flushing during idle times **[minimizes the frequency of cache line flushes initiated by a replacement algorithm so that I/O requests do not have to wait for dirty data in the cache to be written to mass storage and that idle time flushing minimizes the possibility of data loss and performs cache line flushes at an optimal time**

(Column 4, lines 48-56)]. Loechel also teaches that having a system that uses a virtual addressing technique provides a way to **["determine if whether a particular block is contained within the cache at a given time" (Column 5, lines 20-25)]**.

Therefore, it would have been obvious to combine (US 5,943,687) by Liedberg with (US 5,895,488) by Loechel for the benefit of creating a cache flushing system to obtain the invention as specified in claim 13.

48. As per **claim 14**, Liedberg teaches cache flushing based on priority, but fails to expressly discloses that "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space."

Loechel teaches "the selection criteria for a scheme used when there is low demand for cache space is the inverse of the selection criteria used when there is high demand for cache space" as it is taught that **[the cache is flushed if the determined percentage of dirty lines exceeds a predetermined threshold (Abstract, lines 3-4)]**. This condition would encompass a high demand for cache space. Loechel also teaches that **[if the state of the system is determined to be idle, a line of cache is flushed (Abstract, lines 10-12)]**; providing flushing during a low demand period, which encompasses no demand since the state of the system would be idle. Loechel also discloses the existence of a scheme called **["panic flush" when the "amount of dirty cache lines exceeds a predetermined threshold" which equals a period of high demand and of another scheme "one flush line at a time" as disclosed in the invention, which is carried out at idle or low demand periods "and is referred to**

as controlled flushes" (Column 4, lines 57-60)]; providing different and opposite schemes for flushing the cache depending on the demand for cache space.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have different and opposite schemes to flush data from cache when there is high demand and when there is low demand for cache memory space. As explained by Loechel; cache structures may be flushed with a high intensity; a "panic flush" during high demand or one line at a time; "controlled flushes" during idle times.

The motivation for doing so would have been because Loechel teaches that flushing during idle times **[minimizes the frequency of cache line flushes initiated by a replacement algorithm so that I/O requests do not have to wait for dirty data in the cache to be written to mass storage and that idle time flushing minimizes the possibility of data loss and performs cache line flushes at an optimal time (Column 4, lines 48-56)].**

Therefore, it would have been obvious to combine (US 5,895,488) by Loechel with (US 5,943,687) by Liedberg for the benefit of a cache flushing system to obtain the invention as specified in claim 14.

49. As per **claim 15,** Loechel discloses a cache flushing apparatus/system wherein "the higher demand load exists when free space in a cache decreases below a selected free space threshold" **[the cache is flushed when the amount of dirty cache lines exceeds a predetermined threshold (Column 4, lines 57-59)].**

50. As per **claim 18**, Loechel discloses a cache flushing system that "flushes data when a lower demand load comprises substantially no demand" as it is taught that

[flushing a dirty line when the system is determined to be idle (Column 3, lines 38-40)] may be done to improve the general performance of the system.

51. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over Liedberg (US 5,943,687) in view of Loechel (US 5,895,488) as applied to claims 13-15 and 18 above, and further in view of Defouw et al. (US 6,742,084).

As per **claim 16**, the combination of Liedberg as modified by Loechel discloses a cache flushing apparatus/system according to the claimed invention as explained above, but fails to disclose expressly that the apparatus/system includes "a sort module to order the low priority cache structures according to size".

Defouw discloses a cache flushing apparatus/system in which "a sort module is included to order the low priority cache structures according to size". **[Defouw teaches that a data block flushed from the cache will always be the least recently used of all the cached blocks within a given size range (Column 2, lines 56-58 and 61-62)].** Defouw describes a method where data blocks are categorized depending on parameters such as data block size and **[are divided into classes such that all blocks in a given class have the same values of the additional parameters (Column 5, lines 51-53)]** as a method of organizing/sorting cache structures by size or by any other parameter.

Liedberg, Loechel and Defouw are analogous art because they are from the same field of endeavor of cache memory flushing.

The motivation for doing so would have been because Defouw teaches that the motivation of having a sorting module is to **[maximize cache hit ratio, minimize the**

overall mean response time, and minimize the bandwidth consumed by the staging activity (Column 3, lines 18-20)].

Therefore, it would have been obvious to combine (US 5,943,687) by Liedberg with (US 5,895,488) by Loechel and further with (US 6,742,084) by Defouw for the benefit of creating a cache flushing system to obtain the invention as specified in claim16.

VII. RELEVANT ART CITED BY THE EXAMINER

52. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

53. The following references teach a cache memory flushing system based on priority and other cache replacement policies such as least recently used or size algorithms.

U.S. PATENT NUMBER

5,394,531

5,956,744

6,349,365

PG PUB 2004 002 4971

PG PUB 2004 011 7441

PG PUB 2004 01 68028

54. The following reference teaches caching using a sorting module to sort the contents of cache by least recently used and by size.

U.S. PATENT NUMBER

6,629,201

VIII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

55. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) SUBJECT MATTER CONSIDERED ALLOWABLE

56. Per the instant office action, claims 5, 11, 17, and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reasons for allowance of claims 5, 11, 17, and 23 in the instant application is the combination with the inclusion in these claims of the limitation of an apparatus for flushing data from cache to secondary storage wherein "**the first scheme selects a low priority cache structure that will free a greater amount of space in a cache and the second scheme selects a low priority cache structure that will free a lesser amount of space in a cache**." The prior art of record including the disclosures

under section **VII** above neither anticipates nor renders obvious the above recited combination.

a(2) CLAIMS REJECTED IN THE APPLICATION

57. Per the instant office action, claims 1-4, 6-10, 12-16, 18-22, and 24-30 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

58. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:00 AM to 4:30 PM.

IMPORTANT NOTE

59. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR system,

contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 24, 2005

Yaima Campos
Examiner
Art Unit 2185

DONALD SPARKS
SUPERVISORY PATENT EXAMINER